iTPC Electronics & DAQ

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Components

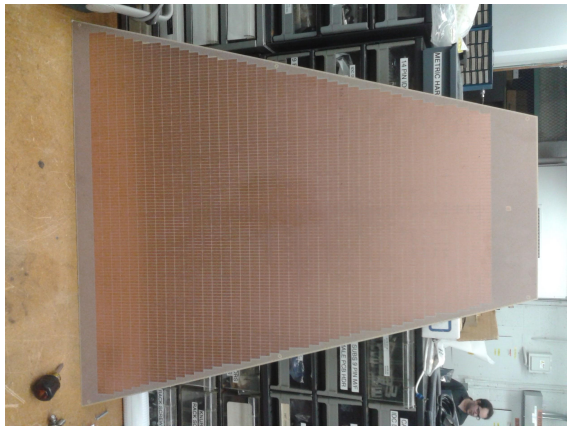
1. Padplane PCB
2. Inner Front End Electronics (iFEE) Boards with SAMPA ASIC
3. Inner ReaDOout (iRDO) Boards
4. Power & Trigger Distribution
5. DAQ Receiver Boards
6. DAQ PCs & Other Components

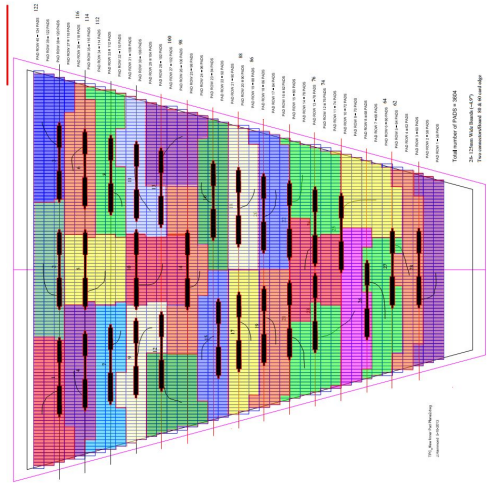
Padplane (1)

- a new padplane needs to be designed & manufactured
  - halogen-free PCB material of large size and large thickness
- first test version (pre-prototype) was designed and manufactured according to old requirements of having electronics only at the edges
  - this doesn't work well due to high capacitive noise because of long traces → no real surprise
  - abandoned due to requirements change → we are now designing according to the current topology of having the iFEE connectors over the entire padplane surface
    - almost the same as the current, old, TPC ⇒ much simpler and safer (risk-free)
- new real prototype is in preparation
  - schematics finished
  - waiting for layout
  - cheaper material

Padplane (2)

- new inner padplane
  - 40 packed rows (vs 13 sparse rows)
  - pad size 5x16 mm (vs 3.35x11.5mm)
  - 3500 pads per sector (vs 1750)
- the number of electronics channels is 2x larger than now ⇒ will represent 50% of the total TPC electronics



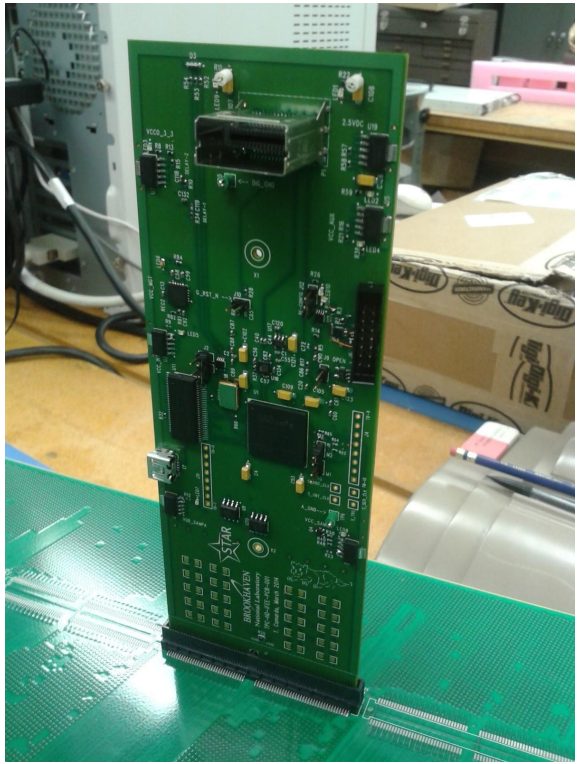


iFEE Overall

- 64 channel device
  - ...compared to the current 32 channel FEE
  - ~same physical size as the old FEE
  - same count of 55 iFEEs per inner sector as the old FEE
    - at roughly the same slot positions
  - same & re-used: mounting brackets, mounting & cooling manifolds → simplifies installation and alleviates risk
  - plugged directly into the new edge connector on the new iTPC padplane
  - will contain
    - 2 x SAMPA ASICs
    - 1 master control FPGA (Spartan 6 series)
    - local voltage regulators and references for the SAMPA
    - connector to the new iRDO readout unit (readout is fast-serial)
    - debugging & local operation: fast USB readout, local FPGA PROM

iFEE (2)

- a pre-prototype exists
  - used to develop firmware and check concepts
    - remote FPGA booting
    - serial links
    - new cable & connector to the new iRDO (SAS based)
    - USB & FPGA PROM for debugging and/or standalone use
  - but has no SAMPA chip
- first real prototype in schematics phase
  - waiting for the SAMPA BGA pinout (Feb 2016)
- testing with SAMPA in the lab in Jun/Jul 2016
- test in TPC with real data from collisions expected in Jan 2017



SAMPA ASIC (1)

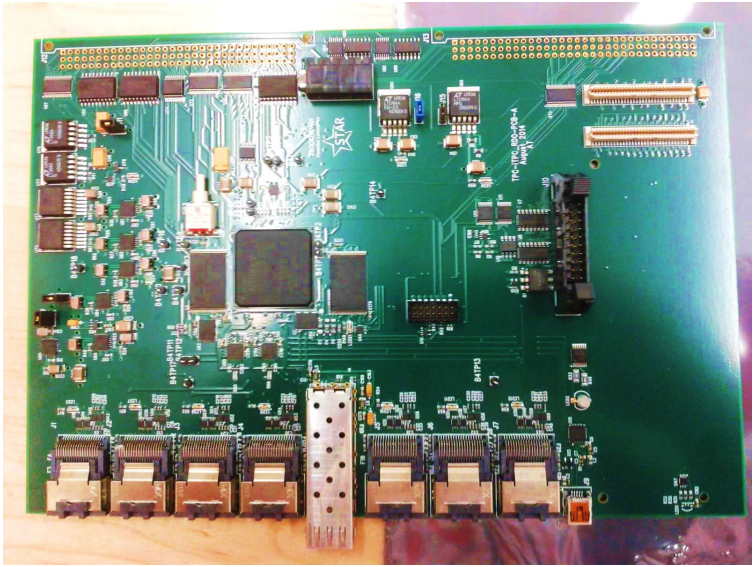
- SAMPA is a 32 channel, integrated pre-amplifier, shaper, ADC, digital filter, zero-suppressor & storage ASIC
- represents an *evolution* from our current STAR & ALICE PASA & ALTRO ASICs with some improvements:
  - 32ch vs 16ch
  - lower power per channel
  - integrated analog preamp-shaper vs separate PASA & ALTRO
  - programmable analog gain, polarity and shaping time (suitable for wires & GEMs)
  - very fast serial readout vs a clumsy 40-lane parallel bus
  - suitable for streaming mode
- designed in Brasil by the Sao Paulo Groups with requirements driven by
  - ALICE TPC Upgrade
  - ALICE MCH Upgrade
  - STAR iTPC Upgrade

SAMPA (2)

- SAMPA Schedule
  - 3 small prototypes finished (so-called MWP1) of:
    - 1 channel analog section, 1 channel ADC, 3 channel ADC+digital section
    - All successful with some issues found & fixed
  - MWP2 is close to being submitted ⇒ expected delivery in May 2016
    - full 32 channel prototype with all the necessary features and also in BGA packaging
    - a critical step
  - MWP3 is scheduled to be submitted in Dec 2016
    - expected to fix bugs and errors discovered (if any) during MWP2 testing…
  - Final Submission in Jan 2018
  - First lot (*fully tested*) Aug 2018
- This is the heart of the iTPC electronics upgrade and is a very crucial component

iRDO (1)

- prototype exists and is currently used to develop firmware



iRDO (2)

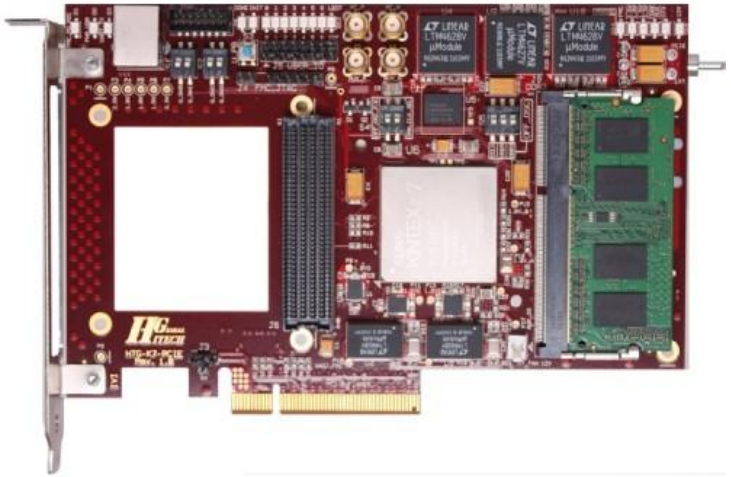
- we expect to stop using the ALICE-developed SIU card (and the corresponding RORC Receiver) and move to internal Xilinx serial channels
  - expect to save $$ because multi-gigabit channels already exist “for free” on the new Xilinx devices (such as e.g. Atrix & Kinetix)
  - decouple ourselves from CERN-developed hardware since CERN is moving in their own specific direction
- in progress...

DAQ Optical Receiver Board (1)

- We have 2 options
  - Use the the ALICE-developed D-RORC custom receiver boards
    - PCIe Based
    - ALICE-developed DDL protocol
    - used in the current TPX
    - somewhat expensive (need to purchase the sender card SIU as well as the receiver D-RORC)
      - ...and the SIU is not really supported anymore...
    - become too closely tied to small CERN-supported companies
      - ...which is becoming an issue...
  - Use direct serial links based upon local protocols and Xilinx cores
    - PCIe Based
    - off-the-shelf
    - with some commercial support e.g. HiTech
- Option 2 is our current default

DAQ Optical Receiver (2)

- off-the-shelf optical receiver candidate
  - supports 10 X 5 Gb/s optical serial channels
    - we plan to use only 4 channels
  - PCIe interface core included
    - will plug into a Linux multi-CPU “DAQ PC”
  - programmable FPGA
    - possible optimizations
- HighTech Xilinx Kintex Dev Kit
- currently under evaluation
  - decision in 2016



Power & Trigger/Clock Distribution

- we plan to re-use the existing 2 power cables per inner sector
  - they exist from the very first TPC electronics thus they are already overspec-ed
  - but we are cautious and will monitor the power use with the prototypes
- power supplies
  - power is somewhat unknown due to the SAMPA
    - but we estimate that the SAMPA is ~1.5x less than the current PASA & ALTRO
    - since we will have 2x more channels we roughly assume that the amount of power needed is almost the same
    - however, the industry is moving to lower voltage thus we will change the existing power supplies
- we plan to re-use existing Trigger TCD cables (PECL standard) for the new inner sector
  - with added connectors

DAQ PCs, fibers etc.

- new DAQ PCs will need to be spec-ed, purchased and installed
  - “usual” Linux boxes with (at least) 8 CPU cores → nothing special these days
- additional optical fibers will need to be installed
  - no particular problem, nothing special…

Cost

	# items	# with spares	$ per item	$ all	With contingency (20%), overhead (56%)
SAMPA	2640	3500	$44	$154k	
iFEE	1320	1580	$130 (wo SAMPA)	$206k	
iRDO	96	116	$1300	$151k	
DAQ Receiver	24	26	$3500	$91k	
Cables, fibers, misc	-	-	-	$50k	
Power Supplies	48	52	$600	$32k	
DAQ PC	24	26	$3000	$80k	
Totals				**$764k**	**$1430k**

Schedule

	2016	2017	2018 early	2018 late
padplane	prototype test produce		start sector installation	end sector installation
iFEE	evaluate SAMPA prototype with SAMPA	final version produce 1 sector's worth	produce all PCBs vet PCB purchase all components install into 1 sector & test	SAMPA arrives mount SAMPA & components Q&A install all full system test
iRDO	prototype 2	final version produce 1 sector's worth	produce & Q&A all install into 1 sector & test	install all full system test
Power Supplies **Trigger Cables** **Fibers**	evaluate	evaluate test	purchase & install all full test using 1 sector's worth	full system test
Receiver Cards	prototype test	final version	purchase & install all full test using 1 sector's worth	full system test
DAQ PCs	develop drivers	final drivers & software... specification	purchase & install all full test using 1 sector's worth	full system test

Risks & Resources

- Manpower is deemed sufficient
  - remark: this same group designed, tested and installed all of the current TPX Electronics (the so-called “DAQ1000 Upgrade”) 8 years ago
- SAMPA is the biggest risk
  - especially related to the delivery schedule (Aug 2018)
    - but → the ASIC will be submitted already in Jan 2018 so we will have ample time to assess possible solutions in case this schedule slips
  - in case of a major schedule slip or major problems with the SAMPA one possibility is to re-use old electronics and readout every 2nd padrow
    - this keeps the Project on schedule but with limited functionality (20 rows vs the required 40, compared to the current 13)

Closing Remarks

- 2016 is a critical year for proof-of-concept prototyping
  - mostly for SAMPA
  - but also the iFEE, iRDO and the DAQ Receiver
  - we must produce the final padplane by July 2016
- 2017 gives us enough time to produce & stress-test final versions of all components (iFEE, iRDO, Receiver Cards, DAQ PC software)
  - we will produce enough electronics for 1 full inner-sector
- 2018 electronics production, Q&A & installation will be tight due to the still “soft” and somewhat unknown SAMPA production schedule
  - we plan to do as much as possible without the SAMPA
    - padplane, iRDOs, Receiver Cards, power supplies, cabling & DAQ PCs can be done earlier
    - iFEE can have the PCB done & vetted earlier